REMARKS

Examiner J. Maldonado is thanked for the thorough examination and search of the subject Patent Application. Claims 1, 9, and 18 have been amended. Claims 4, 5, 13, 14, 16, 17, 22, and 23 have been canceled.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 1-3 and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Huang et al (U.S. 6,180,509) and further in view of Liu (U.S. 5,693,568) is requested based on Amended Claims 1 and on the following remarks.

Applicant has amended Claim 1 to include the limitations previously included in original Claim 5 that has now been canceled. In particular, Amended Claim 1 now reads:

1. (Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tungsten containing film;

depositing a second metal layer overlying said etch stop layer;

etching through said second metal layer, said etch stop layer, and said first metal layer to form connective lines;

thereafter etching through said second metal layer to form vias;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate wherein said dielectric layer is SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), or VT-4 (tetrafluoro-p-xylylene); and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device.

The amendment to Claim 1 now limits the dielectric layer to materials not taught or suggested in the cited prior art. The above amendment is consistent with the original specification and does not constitute new matter.

By comparison, neither Rhodes et al nor Liu teach or suggest the limitation added to Claim 1 by amendment. Applicant believes that amended Claim 1, if entered, will place this claim in condition for allowance with respect to the cited art of Rhodes et al and Liu. Further, Claims 2-3 and 6 represent patentable further limitations on Amended Claims 1 and should not be rejected under 35 U.S.C. 103(a) if Claim 1 is not rejected.

Reconsideration of Claims 1-3 and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Huang et al (U.S. 6,180,509) and further in view of Liu (U.S. 5,693,568) is requested based on Amended Claims 1 and on the above remarks.

Reconsideration of Claims 7 and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over over Rhodes et al (U.S. 4,536,951) in view of Huang et al (U.S. 6,180,509) further in view of Liu (U.S. 5,693,568) and further in view of Wang et al

(U.S. 6,080,660) is requested based on Amended Claim 1 and on the following remarks.

As described above, Applicant has amended Claim 1 to include the limitations previously included in Claim 5. Claim 5 has now been canceled as redundant. Applicant believes that Rhodes et al, Liu, Wang et al, and Huang et al do not teach or suggest the limitation added to Claim 1 by amendment. Claims 7 and 8 represent patentable further limitations on Amended Claims 1 and should not be rejected under 35 U.S.C. 103(a) if Claim 1 is not rejected.

Reconsideration of Claims 7 and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over over Rhodes et al (U.S. 4,536,951) in view of Huang et al (U.S. 6,180,509) further in view of Liu (U.S. 5,693,568) and further in view of Wang et al (U.S. 6,080,660) is requested based on Amended Claim 1 and on the above remarks.

Reconsideration of Claims 9-12 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Ye et al (U.S. 6,080,529) and in view of Liu (U.S. 5,693,568) is requested based on Amended Claim 9 and on the following remarks.

Applicant has amended Claim 9 to include the limitations previously included in original Claim 17 that has now been canceled. In particular, Amended Claim 9 now reads:

9.(Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tantalum containing film;

depositing a second metal layer overlying said etch stop layer;

etching through said second metal layer, said etch stop layer, and said first metal layer to form connective lines;

thereafter etching through said second metal layer to form vias;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate wherein said dielectric layer is SiOF

(fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), or VT-4 (tetrafluoro-p-xylylene); and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.

The amendment to Claim 9 now limits the dielectric layer to materials not taught or suggested in the cited prior art. The above amendment is consistent with the original specification and does not constitute new matter.

By comparison, neither Rhodes et al nor Ye et al nor Liu teach or suggest the limitation added to Claim 9 by amendment. Applicant believes that amended Claim 9, if entered, will place these claims in condition for allowance with respect to the cited art of Rhodes et al and Ye et al and Liu. Further, Claims 10-12 and 15 represent patentable further limitations on Amended Claim 9 and should not be rejected under 35 U.S.C. 103(a) if Claim 9 is not rejected.

Reconsideration of Claims 9-12 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Ye et al (U.S. 6,080,529) and in view of Liu (U.S. 5,693,568) is requested based on Amended Claim 9 and on the above remarks.

Reconsideration of Claims 17-21 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Ye et al (U.S. 6,080,529) and in view of Liu (U.S. 5,693,568) and in view of Wang et al is requested based on Amended Claim 18 and on the following remarks.

Applicant has amended Claim 18 to include the limitations previously included in original Claim 23 that has now been canceled. In particular, Amended Claim 18 now reads:

18. (Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tantalum containing film;

depositing a second metal layer overlying said first metal layer;

depositing an anti-reflective coating layer comprising titanium nitride (TiN) overlying said second metal layer;

etching through said anti-reflective coating layer, said second metal layer, said etch stop layer, and said second metal layer to form connective lines;

thereafter etching through said anti-reflective coating layer and said second metal layer to form vias wherein said etch stop layer acts as an etch stop;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate wherein said dielectric layer is SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), or VT-4 (tetrafluoro-p-xylylene); and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of

the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.

By comparison, neither Rhodes et al nor Ye et al nor Liu nor Wang et al teach or suggest the limitation added to Claim 18 by amendment. Applicant believes that amended Claim 18, if entered, will place these claims in condition for allowance with respect to the cited art of Rhodes et al and Ye and Liu et al and Wang et al. Further, Claims 19-21 represent patentable further limitations on Amended Claim 18 and should not be rejected under 35 U.S.C. 103(a) if Claim 18 is not rejected.

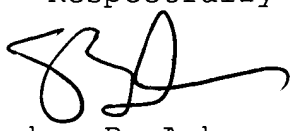
Reconsideration of Claims 17-21 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Ye et al (U.S. 6,080,529) and in view of Liu (U.S. 5,693,568) and in view of Wang et al is requested based on Amended Claim 18 and on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and have discussed their impact on the present invention above.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,



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